Please amend the claims as follows (this listing replaces all prior versions):

1. (Currently Amended) A data recording element for a memory cell of a writable and erasable memory medium comprising:

a laminated structure of at least two multiple-layer structures, each said multiple-layer structure comprising a plurality of individual layers, at least one of [[the]] said plurality of individual layers in each said multiple-layer structure being made of a material capable of changing phase between a crystalline state and an amorphous state in response to an electrical pulse of less than about 10 ns, and one of [[the]] said plurality of individual layers of [[one]] each of said at least two multiple-layer structures having at least one atomic element which is absent from a second one of said plurality of individual layers, wherein said plurality of individual layers of said at least two multiple-layer structures of said laminated structure generates a barrier effect that suppresses an atomic diffusion and reduces a mutual diffusion between said data recording element and other portions of said medium, and

a final individual layer disposed upon said at least two multiple-layer structures, said final individual layer being formed of the same material as a first of said plurality of individual layers [[in]] of a first of said at least two multiple-layer structures of said laminated structure, wherein a crystallization speed of said first of said plurality of individual layers of said first of said at least two multiple-layer structures and said final individual layer is higher than that of other ones of said plurality of individual layers of said ~~first~~ at least two multiple-layer structures and a crystallization temperature of said first of said plurality of individual layers of said first of said at least two multiple-layer structures and said final individual layer is lower that other ones of said plurality of individual layers of said ~~first of said~~ at least two multiple-layer structures.

2. (Currently Amended) The data recording element as recited in claim 1, wherein [[the]] said plurality of individual layers in a first one and a second one of said at least two multiple-layer structures are disposed in a same sequence.

3. (Currently Amended) The data recording element as recited in claim 1, wherein [[the]] said plurality of individual layers in a first one and a second one of said at least two multiple-layer structures are disposed in a different sequence.

4. (Currently Amended) The data recording element as recited in claim 1, wherein each of said plurality of individual layers in each of said at least two multiple-layer structures has a thickness in a range of about 0.1 nm to about 10 nm.

5. (Currently Amended) The data recording element as recited in claim 1, wherein each of [[the]] said plurality of individual layers in each of said at least two multiple-layer structures have the same thickness.

6. (Currently Amended) The data recording element as recited in claim 1, wherein any two adjacent ones of [[the]] said plurality of individual layers ~~in one of said at least two multiple-layers structures~~ have a ratio of thickness of about 0.1 to about 10.

7. (Currently Amended) The data recording element as recited in claim 1, wherein the total thickness of [[the]] said data recording element is in a range of about 5 nm to about 500 nm.

8. (Currently Amended) The data recording element as recited in claim 1, wherein the total thickness of [[the]] said data recording element is in a range of about 5 nm to about 100 nm.

9. (Currently Amended) The data recording element as recited in claim 1, wherein at least one of [[the]] said plurality of individual layers is formed of a material selected from a group consisting of Ge, Te, Sb, GeTe, SbTe, AgIn, GeSbTe, AgInSbTe, TeAsGe, TeSeS, TeSeSb, InSbTe, TeGeSn, In, Cr, N, Se, Sn, Si, Bi, and Ag.

10. (Currently Amended) The data recording element as recited in claim 1, wherein said at least one of [[the]] said plurality of individual layers is deposited in a crystalline state.

11. (Currently Amended) The data recording element as recited in claim 1, wherein a resistance of said at least one of said plurality of individual layers is lower in [[a]] said crystalline state than that in [[an]] said amorphous state.

12. (Canceled)

13. (Canceled)

14. (Currently Amended) The data recording element as recited in claim 1, wherein [[the]] said crystallization temperature of said first ~~of first~~ of said plurality of individual layers [[in]] of said first of said at least two multiple-layer structures of said laminated structure and said final individual layer is in a range of about 90°C to 120°C.

15. (Currently Amended) The data recording element as recited in claim 1, further comprising an electrode formed adjacent ~~to the~~ said data recording element, an edge of [[the]] said electrode contacting [[the]] said data recording element for transferring electrical signals between [[the]] said electrode and [[the]] said data recording element.

16. (Original) The data recording element as recited in claim 1, wherein said laminated structure forms a superlattice-like structure.

17. (Currently Amended) A data recording element for a memory cell of a writable and erasable memory medium comprising:

a laminated structure having a first external layer, a second external layer and a plurality of internal layers formed between [[the]] said first and second external layers, at least one layer of [[the]] said laminated structure being made of a material capable of changing phase between a crystalline state and an amorphous state in response to an electrical pulse of less than about 10 ns, wherein said plurality of individual layers of said at least two multiple-layer structures of said laminated structure generates a barrier effect that suppresses an atomic diffusion and reduces a mutual diffusion between said data recording element and other portions of said medium,

wherein said first and second external layers have a relatively higher crystallization speed and lower crystallization temperature than [[the]] said plurality of internal layers.

18. (Canceled)

19. (Currently Amended) The data recording element as recited in claim 17, wherein [[the]] said crystallization temperature of said first and second external layers is in a range of about 90°C to 120°C.

20. (Currently Amended) A memory cell for a writable and erasable memory medium comprising:

a substrate;

first and second contacts formed on said substrate;

a data recording element formed between said first and second contacts, said data recording element comprising a laminated structure of two or more multiple-layer structures and a final individual layer disposed upon said at least two multiple-layer structures; each of said at least two multiple-layer structures comprising a plurality of sequentially disposed individual layers, at least one of said plurality of sequentially disposed individual layers in each of said at least two multiple-layer structures being a material capable of changing phase between a crystalline state and an amorphous state in response to an electrical pulse of less than about 10 ns, one of [[the]] said plurality of sequentially disposed individual layers having at least one atomic element which is absent from a second one of the plurality of sequentially disposed individual layers, wherein said plurality of sequentially disposed individual layers generates a barrier effect that suppresses an atomic diffusion and reduces a mutual diffusion between said data recording element and other portions of said medium; said final individual layer being formed of the same material as a first of said plurality of sequentially disposed individual layers in a first of said at least two multiple-layer structures of said laminated structure wherein a crystallization speed of said first of said plurality of sequentially disposed individual layers of said first of said at least two multiple-layer structures and said final individual layer is higher than that of other ones of said plurality of sequentially disposed individual layers of said ~~first of said~~ at least two multiple-layer structures and a crystallization temperature of said first of said plurality of sequentially disposed individual layers of said first of said at least two multiple-layer structures and said final individual layer is lower that other ones of said plurality of sequentially disposed individual layers of said ~~first of said~~ at least two multiple-layer structures;

a high temperature electrode formed adjacent [[the]] said data recording element; and

an insulating material isolating said memory cell from adjacent memory cells.

21. (Currently Amended) An electrically writable and erasable memory medium comprising a plurality of memory cells and an arrangement of conductors such that each of said plurality of memory cells is electrically addressable, each said memory cell comprising:

a substrate;

first and second contacts formed on said substrate;

a data recording element formed between said first and second contacts, said data recording element comprising a laminated structure of two or more multiple-layer structures and a final individual layer disposed upon said at least two multiple-layer structures; each of said at least two multiple-layer structures comprising a plurality of sequentially disposed individual layers, at least one of said plurality of sequentially disposed individual layers in each of said at least two multiple-layer structures being a material capable of changing phase between a crystalline state and an amorphous state in response to an electrical pulse of less than about 10 ns; one of [[the]] said plurality of sequentially disposed individual layers having at least one atomic element which is absent from a second one of [[the]] said plurality of sequentially disposed individual layers, wherein said plurality of sequentially disposed individual layers of said at least two multiple-layer structures of said laminated structure generates a barrier effect that suppresses an atomic diffusion and reduces a mutual diffusion between said data recording element and other portions of said medium; said final individual layer being formed of the same material as a first of said plurality of sequentially disposed individual layers in a first of said at least two multiple-layer structures of said laminated structure wherein a crystallization speed of said first of said plurality of sequentially disposed individual layers of said first of said at least two multiple-layer structures and said final individual layer is higher than that of other ones of said plurality of sequentially disposed individual layers of said ~~first of said~~ at least two multiple-layer structures and a crystallization temperature of said first of said plurality of sequentially disposed individual layers of said first of said at least two multiple-layer structures and said final individual layer is lower that other ones of said plurality of sequentially disposed individual layers of said ~~first of said~~ at least two multiple-layer structures;

a high temperature electrode formed adjacent [[the]] said data recording element; and

an insulating material isolating said memory cell from adjacent memory cells.

22. (Withdrawn) A method of producing a data recording element for a memory cell of electrically writeable and erasable memory medium, the method comprising:

depositing a first multiple-layer structure on a substrate; said multiple-layer structure consisting of at least two individual layers, at least one of said individual layers being a material capable of changing phase between a crystalline state and an amorphous state in response to an electrical pulse;

depositing one or more further multiple-layer structures on said first multiple-layer structure to form a laminated structure, said further multiple-layer structures comprising at least two individual layers, at least one of said individual layers being a material capable of changing phase between a crystalline state and an amorphous state in response to an electrical pulse,

wherein one individual layer of said first and further multiple layer structures having at least one atomic element which is absent from another individual layer.

23. (Withdrawn) The method as recited in claim 22, further comprising depositing a final individual layer formed of a same material as a first individual layer of said first multiple-layer structure.

24. (Withdrawn) The method as recited in claim 23, wherein said first and final individual layers having a relatively high crystallization speed and low crystallization temperature than other layers of the first and further multiple-layer structure.

25. (Withdrawn) The data recording element as recited in claim 24, wherein the crystallization temperature of said first and final individual layers is in a range of about 90°C to 120°C.

26. (Withdrawn) A method of producing a memory cell for a writeable and erasable memory medium, comprising:

depositing an insulating material on a substrate;

depositing a first contact on said insulating material;

depositing a high temperature electrode adjacent said first contact;

sequentially depositing two or more multiple-layer structures to form a data recording element, each said multiple-layer structure comprising two or more individual layers, at least one said individual layer in each said multiple-layer structure being formed from a material capable of changing phase between a crystalline state and an amorphous state in response to an electrical pulse; one of the plurality of individual layers having at least one atomic element which is absent from other one of the plurality of individual layers;

depositing a second contact on said data recording element; and

depositing further insulating material to isolate said memory cell from adjacent memory cells.

27. (Withdrawn) The method as recited in claim 26, further comprising depositing a final individual layer formed of a same material as a first individual layer of said first multiple-layer structure.

28. (Withdrawn) A method of writing and erasing information to an electrically writeable and erasable memory medium having a plurality of memory cells and an arrangement of conductors such that each memory cell is electrically addressable, each memory cell comprising:

a substrate;

first and second contacts formed on said substrate;

a data recording element formed between said first and second contacts, said data recording element having a laminated structure of two or more multiple-layer structures, each said multiple-layer structure having a plurality of sequentially disposed individual layers, at least one of said individual layers in each multiple-layer structure being a phase-change material capable of changing phase between a crystalline state and an amorphous state in response to an electrical pulse, one of the plurality of individual layers having at least one atomic element which is absent from other one of the plurality of individual layers.; and

a high temperature electrode formed adjacent the data recording element;

the method including:

applying an energy pulse to said data recording element via said high temperature electrode, said energy pulse supplying sufficient energy to change said phase-change material between a crystalline phase and an amorphous phase.

29. (Withdrawn) The method as recited in claim 28, wherein said energy pulse is a single pulse.

30. (Withdrawn) The method as recited in claim 28, wherein said energy pulse is a chain of multi-pulses.

31. (Withdrawn) The method as recited in claim 28, wherein said energy pulse has a duration of less than about 50 ns for data writing.

32. (Withdrawn) The method as recited in claim 30, wherein said energy pulse has a duration of not more than 7 ns for data writing.

33. (Withdrawn) The method as recited in claim 28, wherein said energy pulse has a duration of less than about 50 ns for data erasing.

34. (Withdrawn) The method as recited in claim 32, wherein said energy pulse has a duration of not more than about 10 ns for data erasing.